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10/046,077	01/16/2002	Hiroshi Inagawa	XA-9612	2431

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,077	INAGAWA ET AL.	
	Examiner	Art Unit	
	David S Blum	2813	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-17* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

This action is in response to election paper #6, filed 10/14/03.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-17 in Paper No. 6 is acknowledged.

2. Claims 18-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

Specification

3. Claims 4, 5 and 8 are objected to because of the following informalities: claims 4, 5, and 8 recite "said conductive layer owns a pillar". The examiner believes "owns" is a typographical error Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 limits the device to having a first electrode between a side wall spacer and the same side wall spacer. It is unclear how this exists.

Claim 17 limits the side wall to being formed via thermal oxidation. Although in a device claim, the method of forming the layer is given no patentable weight (discussed below), this still presents an issue as the side wall is of silicon and silicon oxide, not all silicon oxide. The applicant may have meant "the side wall spacer".

6. Claim 9 recites the limitation "said second electrode" in the device. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 4, 6-7, 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu (US005396093A).

Lu teaches the device of claims 1, 4, 6-7, 12-17 in that:

Claim 1. An insulated-gate type semiconductor device in which a conductive layer (28) for a gate (24) is embedded into a trench (figure 8B) which is formed in a semiconductor substrate (12), and a conductive layer (52) for a source is provided on a major surface of said semiconductor substrate, wherein:

a portion of a gate pillar which is constituted by both said conductive layer (52) for said gate and a cap insulating film (24) for capping an upper surface of said conductive layer for said gate is projected from the major surface (figure 8B) of said semiconductor substrate;

a side wall spacer (32) is provided on a side wall of said projected portion of the gate pillar; and

said conductive layer (52) for said source is connected to a contact region of the major surface of the semiconductor substrate, which is defined by said side wall spacer (figure 8B).

Claim 4. An insulated-gate type semiconductor device comprising:

first semiconductor region selectively formed in a semiconductor substrate; (figure 3A)

a second semiconductor region selectively formed in said first semiconductor region (figure 3A);

a trench (14) which is reached from a major surface of said second semiconductor region to said semiconductor substrate; and

a conductive layer (28) which is formed via (18) an insulating film in said trench;

wherein:

a gate pillar which is constituted by said conductive layer (28) and a cap insulating film (24) for capping an upper surface of said conductive layer owns a pillar which is elongated on a major surface of said second semiconductor region; (figure 6B)

a side wall (32) spacer is provided on a side wall of the pillar of said gate pillar;

an electrode (52) is connected to said second semiconductor region in a contact region which is defined by said side wall spacer (figure 9B); and

said semiconductor substrate is used as a drain (8), said conductive layer is used as a gate, and said second semiconductor region is used as a source (30).

Claim 6. An insulated-gate type semiconductor device as claimed in claim 4 wherein: said conductive layer which constitutes the gate is polycrystal silicon (conductive layer is made of doped poycrystal silicon, column 4 lines 65-68); and said insulating film is an oxide film (column 5 lines 4-5, oxide).

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113 thus, the part need only be oxide, not a thermal oxide.

Claim 7 (as best understood by the examiner). An insulated-gate type semiconductor device comprising,:

a first conductivity type semiconductor main body (10, N+);

a second conductivity type first semiconductor (12, P-) region formed at a predetermined depth (figure 9B) within one major surface of said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region (30 N+) formed at a predetermined depth within said first semiconductor region;

a first trench (14) which penetrates said first semiconductor region, and is reached from a major surface of said second semiconductor region to said semiconductor main body;
a pillar gate which is constituted by both a gate-purpose conductive layer (28) embedded via an insulating film (18) into said first trench and a cap insulating film (24) for capping an upper surface of said gate-purpose conductive layer, and a portion of which pillar gate having a pillar portion projected from the major surface of said second semiconductor region (figure 9B); and
a first electrode (52) which is electrically connected to said second semiconductor region in a region between a side wall spacer (32) provided on a side wall of said pillar portion of the pillar gate, and said side wall spacer.

Claim 12. An insulated-gate type semiconductor device as claimed in claim 7 wherein: said first trenches are formed in a stripe shape in such a manner that a side surface of said first semiconductor region constitutes either a crystalline surface (100) or a surface equivalent to said crystalline surface (100), and carriers are moved along either said crystalline surface (100) or said surface equivalent to said crystalline surface (100) by an electric field of said conductive layer for said gate. (figure 7 shows trenches in stripe shape. Lu is silent as to crystal orientation. The surface is monocrystal, thus crystalline (column 3 line 45) and therefore, the trenches are in a 001 or equivalent surface and carriers move along the surface.

Claim 13. An insulated-gate type semiconductor device

as claimed in claim 7 wherein:

a field insulating film is formed (16)on a portion of the major surface of said semiconductor main body;

an extension portion of said conductive layer for said gate is provided on a portion of said field insulating film (figure9B); and

a third electrode (also 52 or 56) made of the same material as that of said first electrode is connected to said extension portion of said conductive layer for said gate. (part 52 may be the first and third electrode and read on the claim limitation)

Claim 14. An insulated-gate type semiconductor device as claimed in claim 13 wherein;

A back to back protective element (54) which is electrically connected between said first electrode (52) and said third electrode (56) is provided on another portion of said field insulating film.

Claim 15. An insulated-gate type semiconductor device having a longitudinal structure, comprising:

a semiconductor main body indicative of a first conductivity type (10);

a first semiconductor region indicative of a second conductivity type (12), which is formed in said semiconductor main body;

a second semiconductor region indicative of the first conductivity type (30), which is formed in said first semiconductor region; and

a trench gate (28) which is reached from a major surface of said second semiconductor region to the region of said semiconductor main body; wherein:

a portion of a gate pillar which is made of both said trench gate (28) and an insulating film (24) for covering an upper surface of said trench gate exceeds and is projected from the major surface of said second semiconductor region (figure 9B);

a side wall spacer (32) is provided on a side wall of said projected gate pillar; and

a source electrode connected to said semiconductor region is provided on a contact region defined by said side wall spacer (figure 9B).

Claim 16. An insulated-gate type semiconductor device having a longitudinal structure, comprising:

a semiconductor main body indicative of a first conductivity type (10);

a first semiconductor region indicative of a second conductivity type (12), which is formed in said semiconductor main body;

a second semiconductor region (30) indicative of the first conductivity type, which is formed in said first semiconductor region; and

trench gate (28) which is reached from a major surface of said second semiconductor region to the region of said semiconductor main body; wherein:

a portion of said trench gate exceeds and is projected from the major surface of said second semiconductor region (figure 9B);

a side wall spacer (32) is provided on both said projected trench gate and a side wall of an insulating film for covering an upper surface of said trench gate; and

a source electrode (52)connected to said semiconductor region is provided in a contact hole defined by said side wall spacer (figure 9B).

Claim 17. An insulated-gate type semiconductor device as claimed in claim 15 wherein:

said side wall is formed via a thermal oxidation film which is formed on a surface of the projected portion of said trench gate. Insulating film is an oxide film (column 5 lines 4-5, oxide).

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113 thus, the part need only be oxide, not a thermal oxide.

Claim Rejections - 35 USC § 103

9. Claims 2, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (US005396093A) in view of Huang (US006437399B1).

Lu teaches the device of claims 2, 5 and 8, except for the conductive layer for the source being embedded into the substrate.

Claim 2. An insulated-gate type semiconductor device in which said conductive layer Lu, 52, not embedded into a trench) for said source is embedded into a trench which is

formed in a semiconductor substrate, and said conductive layer for said source is provided on a major surface of said semiconductor substrate (figure 9B), wherein:
a portion of a gate-portion conductor (28)layer is projected from the major surface of said semiconductor substrate;
a side wall spacer (32) is provided on both a side wall of said projected conductive layer and a side wall of a cap (24) insulating film for capping an upper surface
of said conductive layer for said gate; and
said conductive layer for said source is formed in a source contact hole (Lu, space, but not hole defined by spacer) which is defined by said side wall spacer.
Huang teaches the conductive layer for said source is embedded into a trench which is formed in a semiconductor substrate, and said conductive layer for said source is provided on a major surface of said semiconductor substrate (figure 13). Metal layer 36 is formed to establish contact. Huang teaches that this makes alignment easier, the only alignment required is to contact the trench (column 2 lines 39-43).

Claim 5. An insulated-gate type semiconductor device comprising:
a first semiconductor region selectively formed in semiconductor substrate (figures 4 and 7);
a second semiconductor region selectively formed in said first semiconductor region (figures 4 and 7);
a trench (figure 3A) which is reached from a major surface of said second semiconductor region to said semiconductor substrate; and

a conductive layer (28) which is formed via an insulating film (18) in said trench;

wherein:

a portion of said conductive layer (28) owns a pillar which is elongated on a major surface of said second semiconductor region (figure 6B);

a side wall spacer (32) is provided on both a side wall of the pillar of said conductive layer and also a side wall of a cap insulating film (24) for capping an upper surface of said conductive layer (figure 9B);

an electrode is connected to said second semiconductor region in a contact hole (Lu, space, but not hole defined by spacer) formed in a contact region which is defined by said side wall spacer; and

said semiconductor substrate is used as a drain (8), said conductive layer is used as a gate, and said second semiconductor region is used as a source (30).

Huang teaches the conductive layer for said source is embedded into a trench which is formed in a semiconductor substrate, and said conductive layer for said source is provided on a major surface of said semiconductor substrate (figure 13). Metal layer 36 is formed to establish contact. Huang teaches that this makes alignment easier, the only alignment required is to contact the trench (column 2 lines 39-43).

Regarding the functional language of claim 5 "used as", a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be used does not differentiate the claimed apparatus from the prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim Ex parte Masham, 2

USPQ2d 1647 (Bd. Pat. App.& Inter. 1987) MPEP 2114. The corresponding parts of Lu and Huang are as (same function) in the instant application.

Claim 8. An insulated-gate type semiconductor device comprising:

a first conductivity type (10) semiconductor main body;

a second conductivity type first semiconductor (12) region formed at a predetermined depth within one major surface of said semiconductor main body, said second conductivity type being opposite to said first conductivity type (figure 9B);

first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region (30);

a plurality of first trenches (figures 3A and 4) which penetrates said first semiconductor region, and are reached from a major surface of said second semiconductor region to said semiconductor main body;

a conductive layer for a gate embedded (28) via an insulating film (18) into each of said first plural trenches, and a portion of which said conductive layer for said gate owns a pillar portion projected from the major surface of said second semiconductor region (figure 9B);

side wall spacers (32) provided on a side wall of said pillar portion and also a side wall of a cap insulating film (24) for capping an upper surface of said pillar portion;

a plurality of second trenches which are made shallower than said first trenches (Huang shows these trenches to be either shallower (figures 9 and 11) or deeper (figure 13), and are formed in such a manner that said second trenches are reached

from the major surface of the second semiconductor region to said first semiconductor region between said side wall spacers located adjacent to each other; and

first electrode which is embedded into each of said second trenches so as to be electrically connected to said first semiconductor region and said second semiconductor region (figures 9 and 11), and which is commonly connected on said conductive layer for said gate.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Lu by contacting the source in a trench as taught by Huang to make alignment easier.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (US005396093A) in view of Wolf (page 384).

Lu teaches the device of claim 3 except for the conductive layer for the source containing aluminum.

Claim 3. An insulated-gate type semiconductor device as claimed in claim 1 wherein:

said conductive layer for said gate is made of polycrystal silicon containing an impurity (column 4 lines 65-68); and

said conductive layer for said source is made of a metal which contains aluminum as a major component.

Lu teaches the conductive layer for the source of conductive silicon. Wolf (page 384) teaches contacts may be made of silicon or replaced by aluminum or a refractory metal, teaching an art recognized equivalence.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Lu by substituting aluminum for the silicon contact as taught by Wolf to be an art recognized equivalent.

11. Claim 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu (US005396093A) in view of Wolf (page 384).

Lu teaches the device of claim 9 (as described above in regard to claim 7), except for the conductive layer for the source containing aluminum.

Claim 9. An insulated-gate type semiconductor device

as claimed in claim 7 wherein:

said conductive layer for said gate is made of polycrystal silicon containing an impurity (column 4 lines 65-68);

said first electrode is made of a metal which contains aluminum as a major component; and

said second electrode is made of a metal material different from said metal material of the first electrode.

Lu teaches the conductive layer for the source of conductive silicon. Wolf (page 384) teaches contacts may be made of silicon or replaced by aluminum or a refractory metal, teaching an art recognized equivalence. Lu also teaches a second electrode (56, part of capacitor electrode) to be silicon of a different doping level than the second electrode. Thus Lu teaches the first and second electrode to be of different materials.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Lu by substituting aluminum for the silicon contact as taught by Wolf to be an art recognized equivalent.

Allowable Subject Matter

12. Claims 10, 11, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 limits the device to having a second electrode on the opposite surface to the major surface (thus an electrode on the bottom of the substrate). Lu has a dopes layer at this location, but does not teach or suggest a contact that would make this layer an electrode (or drain as in claim 11). Huang does not suggest any modification for this electrode.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (703)-306-9168 and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (703)-308-4940. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317. Our receptionist's number is (703)-308-0956.

David S. Blum

November 18, 2003